IN THE SPECIFICATION:

Please amend the specification as follows:

On pages 3-4, please replace paragraphs the last three paragraphs of page 3 as follows:

-- As depicted in Figure 2, the timing requirements of the top-level design are used in the present invention to form a time-budget for the system, as depicted by block 26. Time-budgeting is a process of defining all of the timing requirements of input and output signals of each sub-module design to achieve functional operability as well as speed of operation of the top-level design. Hence, the time-budget 26 process provides the timing for the different sub-modules A, B, C. This is depicted in the synthesis of Figure 2 by blocks 28A, 28B and 28C. The timing requirements of sub-modules A, B, C, provided in blocks 28A, 28B and 28C, are used in the synthesis process of each of the individual sub-modules.

The top-level RTL is broken down into 3 logical RTL blocks, sub-module A RTL, sub-module B RTL and sub-module C RTL. These are represented by blocks 30A, 30B and 30C in Figure 2. With the input of the timing requirements for the individual sub-module, and the sub-module RTL, broken down from the top-level RTL, a synthesis of each sub-module as a stand-alone design is performed as depicted in blocks 32A, 32B and 32C. The synthesis process of an individual sub-module will be described later with respect to Figure 3. The synthesis of each sub-module design is performed independently, and generates a stand-alone design. Such a synthesis is performed in accordance with conventional RTL and synthesis techniques for the individual sub-module designs.

Each sub-module A, B, C undergoes an iterative process in order to meet the timing requirements of its input and output signals. Once a static timing analysis performed on each sub-module design verifies the timing requirements, a sub-module netlist is produced, as

depicted in blocks 34A, 34B and 34C. The netlist is a list of components and connections for the sub-modules.--

On page 4, please replace paragraph 3 as follows:

-- Figure 3 depicts a typical flow of the synthesis of an RTL-based design for a sub-module, as depicted by blocks 32A, 32B and 32C in Figure 2. This synthesis of an RTL-based design may be used for top-level designs or for individual sub-module designs. The synthesis finds particular application in the present invention for synthesizing sub-modules, which are then integratable into a top-level design, rather than using the synthesis to directly synthesize the top-level design.--

On page 5, please replace paragraphs 2 and 3 as follows:

-- The procedures described above are summarized in the flow chart of Figure 4 in which the top-level timing requirements are provided in step 60. The time-budget of each of the sub-modules determines the timing requirements for each of the sub-modules, as provided in step 62. Each of the sub-modules undergoes independent gate-level synthesis in steps 64A-C. The gate-level synthesis for the sub-module design is based on the timing requirements, wire load modules, and I/O signal loadings, for example. Verification of the performance of the gate-level design of the sub-modules are performed in steps 65A-C. These include static timing analysis, dynamic simulations and other formal verifications. It is then determined in steps 66A-C. for each of the sub-modules whether the timing requirements for the sub-modules are met. If they are not met, the synthesis process for the individual sub-module or sub-modules are performed until the timing requirements are met and verifications passed.